

HDMI Companion Chip with I²C Level Shifting Buffer, 12 Channel ESD, and Current-Limit Load Switch

Check for Samples: [TPD12S016](#)

FEATURES

- Confirms to HDMI Compliance Tests without any External Components
- Supports HDMI1.4 Data Rate
- Match Class D and Class C Pin Mapping
- 8-Channel ESD Lines for Four Differential Pairs with Ultra-low Differential Capacitance Matching (0.05pF)
- On-chip Load Switch with 55mA Current Limit Feature at the HDMI 5V_OUT Pin
- Auto-direction Sensing I²C Level Shifter with One-shot Circuit to Drive Long HDMI Cable (750pF Load)
- Back-drive Protection on HDMI Connector Side Ports

- Integrated Pull-up and Pull-down Resistors per HDMI Specification
- ±8KV Contact Discharge Rating at all External Pins
- Space Saving 24-pin RKT Package and 24-TSSOP Package

APPLICATIONS

- Cell Phones
- eBook
- Portable Media Players
- Set-top Box

DESCRIPTION

The TPD12S016 is a single-chip HDMI interface device with auto-direction sensing I²C voltage level shift buffers, load switch, and integrated high-speed ESD protection clamps. The device pin mapping matches the HDMI Type D connector with four differential pairs. This device offers eight low-capacitance ESD clamps, allowing HDMI 1.4 data rates. The integrated ESD circuits provide good matching between each differential signal pair, which allows an advantage over discrete ESD solutions where variations between ESD protection clamps degrade the differential signal quality. The TPD12S016 provides a current limited 5 V output (5V_OUT) for sourcing the HDMI power line. The current limited 5 V output supplies up to 55 mA to the HDMI receiver. The control of 5V_OUT and the hot plug detect (HPD) circuitry is independent of the LS_OE control signal, and is controlled by the CT_HPDP pin. This independent CT_HPDP control enables the detection scheme (5V_OUT and HPD) to be active before enabling the HDMI link. An internal 3.3V node powers the CEC pin eliminating the need for a 3.3V supply on board.

The TPD12S016 integrates all the external termination resistors at the HPD, CEC, SCL, and SDA lines. There are three non-inverting bi-directional translation circuits for the SDA, SCL, and CEC lines. Each have a common power rail (VCCA) on the A side from 1.1 V to 3.6V. On the B side, the SCL_B and SDA_B each have an internal 1.75 kΩ pull up connected to the 5 V rail (5V_OUT). The SCL and SDA pins meet the I²C specification and drive up to 750 pF capacitive loads exceeding the HDMI1.4 specifications. The CEC_B pin has an internal 27 kΩ pull up to the internal 3.3 V supply rail. The HPD_B port has a glitch filter to avoid false detection due to plug bouncing during the HDMI connector insertion.

The TPD12S016 offers reverse current block feature at the 5V_OUT pin. In the fault conditions, such as when two HDMI transmitters connect to the same HDMI cable, the TPD12S016 ensures that the system is safe from powering up through external HDMI transmitter. The Dx, CLKx, SCL_B, SDA_B, CEC_B pins also feature reverse-current blocking when the system is powered off.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TPD12S016

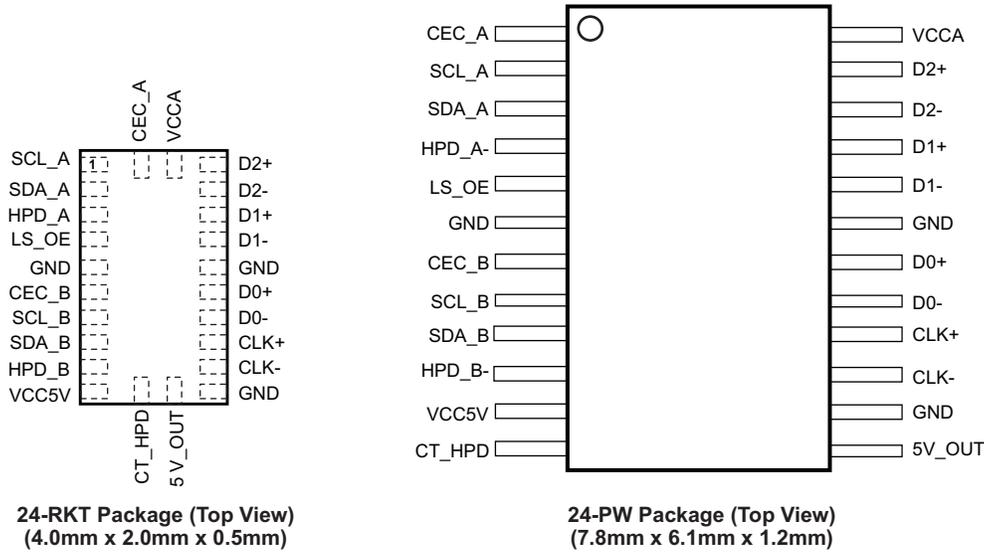
SLLSE96A – SEPTEMBER 2011 – REVISED OCTOBER 2011

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE INFORMATION



APPLICATION INFORMATION

Application Case #1: HDMI Driver Chip is controlling the TPD12S016 via only one control line (CT_HPDP). In this mode the HPD_A to LS_OE pin are connected as shown in the oval dotted line of [Figure 1](#).

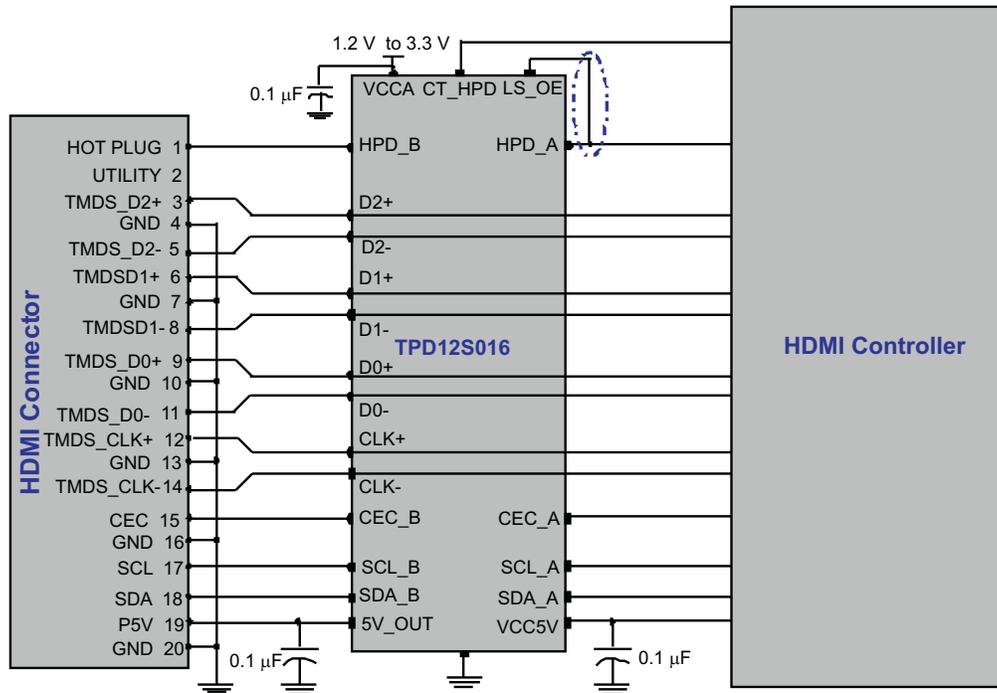


Figure 1. Application Schematics for HDMI Controllers with One GPIO for HDMI Interface Control

Application Case #2: Some HDMI driver chips may have two GPIOs to control the HDMI interface chip. In this case a flexible power saving mode can be implemented.

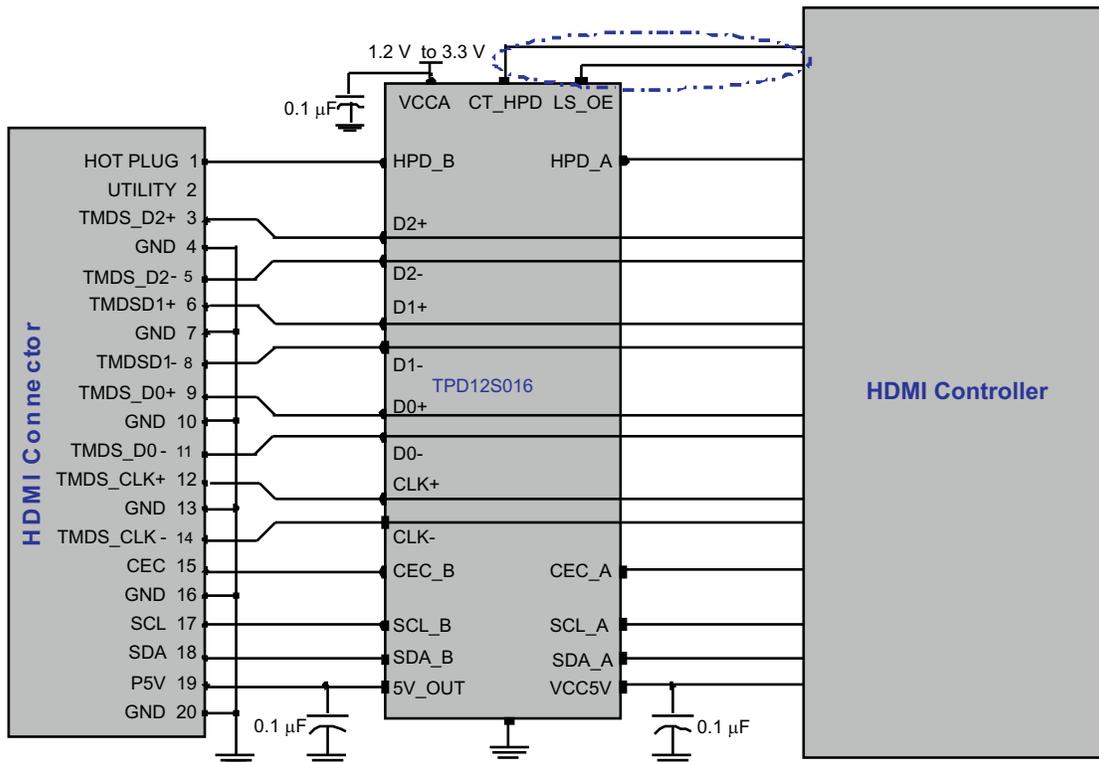


Figure 2. Application Schematics for HDMI Controllers with Two GPIOs for HDMI Interface Control

The LS_OE and CT_HPDP are active-high enable pins. They control the TPD12S016 power saving options according to the following table:

LS_OE	CT_HPDP	VCCA	5V_OUT	A-side Pull-ups	DDC, B-Side Pull-ups	CEC_B Pull-ups	CEC LDO	Load SW and HPD	DDC/ CEC VLTs	ICCA Typ	ICC5V Typ	Comments
L	L	1.8V	5.0V	Off	Off	Off	Off	Off	Off	1 μA	1 μA	Fully Disabled
L	H	1.8V	5.0V	On	On	Off	Off	On	Off	1 μA	30 μA	Load Switch on
H	L	1.8V	5.0V	Off	Off	Off	Off	Off	Off	1 μA	1 μA	Not Valid State
H	H	1.8V	5.0V	On	On	On	On	On	On	13 μA	200 μA	Fully On
X	X	0V	0V	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	X	1.8V	0V	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down
X	X	0V	5.0V	High-Z	High-Z	High-Z	Off	Off	Off	0	0	Power Down

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN –0.4-mm pitch (4.0mm x 2.0mm x 0.5mm)	Tape and reel	TPD12S016RKTR	PN016
	TSSOP –0.65-mm pitch (7.8mm x 6.4mm x 1.2mm)	Tape and reel	TPD12S016PWR	PN016

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

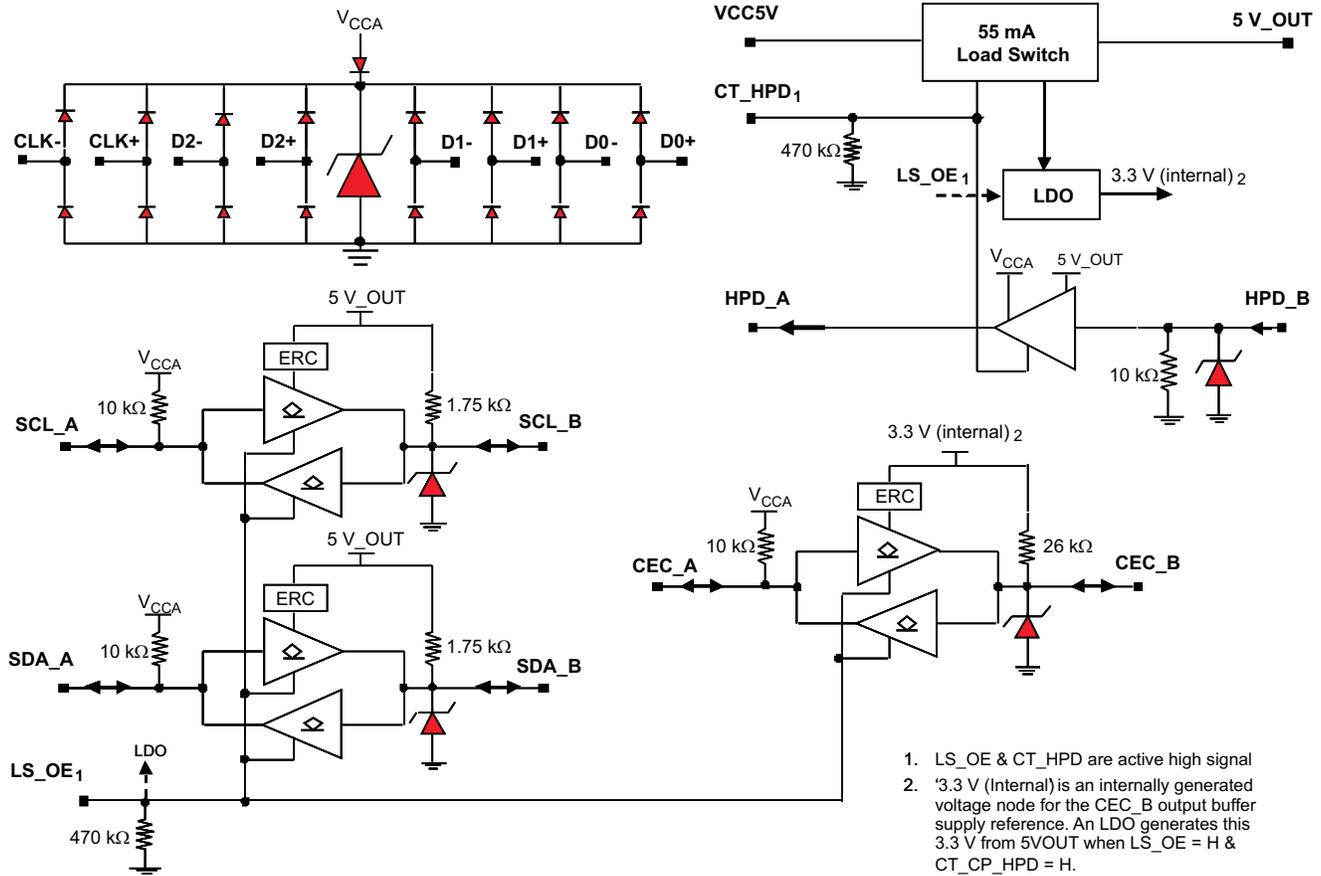
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

TPD12S016

SLLSE96A – SEPTEMBER 2011 – REVISED OCTOBER 2011

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CIRCUIT SCHEMATIC DIAGRAM



PIN FUNCTIONS

PIN			PIN TYPE	DESCRIPTION
NAME	RKT	PW		
D-, D+	16, 17, 19-22	17, 18, 20-23	ESD Terminal	HDMI TMDS Data. Connect to HDMI Controller and HDMI Connector directly.
CLK+, CLK-	14, 15	15, 16	ESD Terminal	HDMI TMDS Clock. Connect to HDMI Controller and HDMI Connector directly.
HPD_A	3	4	Output	Hot plug detect Output referenced to VCCA. Connect to HDMI controller Hot plug detect input pin
HPD_B	9	10	Input	Hot plug detect Input. Connect directly to HDMI Connector Hot Plug Detect pin
CEC_A	24	1	IO Port	HDMI controller side CEC signal pin referenced to VCCA. Connect to HDMI controller.
CEC_B	6	7	IO Port	HDMI connector side CEC signal pin referenced to internal 3.3V supply. Connect to HDMI connector CEC pin.
SCL_A	1	2	IO Port	HDMI controller side SCL signal pin referenced to VCCA. Connect to HDMI controller.
SCL_B	7	8	IO Port	HDMI connector side SCL signal pin referenced to 5V_OUT supply. Connect to HDMI connector SCL pin.
SDA_A	2	3	IO Port	HDMI controller side SDA signal pin referenced to VCCA. Connect to HDMI controller.
SDA_B	8	9	IO Port	HDMI connector side SDA signal pin referenced to 5V_OUT supply. Connect to HDMI connector SDA pin.
LS_OE	4	5	Control Input	Disables the Level shifters when OE =L. The OE pin is referenced to VCCA
CT_HPDP	11	12	Control Input	Disables the load switch and HPD_B when CT_HPDP =L. The CT_HPDP is referenced to VCCA
VCC5V	10	11	Input Power	Internal 5V Supply. (Input to the load switch.)
VCCA	23	24	Input Power	Internal PCB Low Voltage Supply (Same as the HDMI Controller Chip Supply)
5V_OUT	12	13	Output Power	External 5V Supply. (Output of the load switch.)
GND	5, 13, 18	6, 14, 19	Ground	Connect to System Ground Plane

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT	
		MIN	MAX		
V _{CCA}	Supply voltage range	-0.3	4.0	V	
V _{CC5V}	Supply voltage range	-0.3	6.0	V	
V _I	Input voltage range ⁽²⁾	SCL_A, SDA_A, CEC_A	-0.3	4.0	V
		SCL_B, SDA_B, CEC_B	-0.3	6.0	
		CT_HPDP, LS_OE	-0.3	4.0	
		D, CLK	-0.3	6.0	
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	SCL_A, SDA_A, CEC_A, CT_HPDP, LS_OE	-0.3	4.0	V
		SCL_B, SDA_B, CEC_B	-0.3	6.0	
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	SCL_A, SDA_A, CEC_A, CT_HPDP, LS_OE	-0.3	V _{CCA} + 0.5	V
		SCL_B, SDA_B, CEC_B	-0.3	V _{CCB} + 0.5	
I _{IK}	Input clamp current	VI < 0		-50	mA
I _{OK}	Output clamp current	VO < 0		-50	mA
	Continuous current through V _{CCB} , or GND			±100	mA
T _{stg}	Storage temperature range	-65	150	°C	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{CCA}	Supply voltage	1.1		3.6	V
V _{CC5V}	Supply voltage	4.5		5.5	V
V _{IH}	High-level input voltage	SCL_A, SDA_A	V _{CCA} = 1.1V to 3.6 V	0.7×V _{CCA}	V _{CCA}
		CEC_A	V _{CCA} = 1.1V to 3.6 V	0.7×V _{CCA}	V _{CCA}
		CT_HPDP, LS_OE	V _{CCA} = 1.1V to 3.6 V	1.0	V _{CCA}
		SCL_B, SDA_B	5V_OUT = 5.0 V	0.7×5V_OUT	5V_OUT
		CEC_B	5V_OUT = 5.0 V	0.7×V _{3P3} ⁽¹⁾	V _{3P3}
		HPD_B	5V_OUT = 5.0 V	2.0	5V_OUT
V _{IL}	Low-level input voltage	SCL_A, SDA_A	V _{CCA} = 1.1V to 3.6 V	-0.5	0.082×V _{CCA}
		CEC_A	V _{CCA} = 1.1V to 3.6 V	-0.5	0.082×V _{CCA}
		CT_HPDP, LS_OE	V _{CCA} = 1.1V to 3.6 V	-0.5	0.4
		SCL_B, SDA_B	5V_OUT = 5.0 V	-0.5	0.3×5V_OUT
		CEC_B	5V_OUT = 5.0 V	-0.5	0.3×V _{3P3}
		HPD_B	5V_OUT = 5.0 V	0	0.8
V _{ILC}	(contention) Low-level input voltage	SCL_A, SDA_A, CEC_A	V _{CCA} = 1.1V to 3.6 V	-0.5	0.065×V _{CCA}
V _{OL} - V _{ILC}	Delta between V _{OL} and V _{ILC}	SCL_A, SDA_A, CEC_A	V _{CCA} = 1.1V to 3.6 V	0.1×V _{CCA}	mV
T _A	Operating free-air temperature	-40		85	°C

(1) The V3P3 is an internal 3.3V power supply node. The V3P3 is generated from the 5V supply pin through the on-chip LDO.

ESD TABLE

PARAMETER	SIGNALS	TYP	UNIT
HBM ESD	LS_OE, CT_HPDP, SCL_A, SDA_A, CEC_A, HPD_A, V _{CCA}	±2	kV
	Dx, CLKx, SCL_B, SDA_B, CEC_B, HPD_B, 5V_OUT	±15	kV

TPD12S016

SLLSE96A – SEPTEMBER 2011 – REVISED OCTOBER 2011

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ESD TABLE (continued)

PARAMETER	SIGNALS	TYP	UNIT
IEC 61000-4-2 Contact Discharge	Dx, CLKx, SCL_B, SDA_B, CEC_B, HPD_B, 5V_OUT	±8	kV

ELECTRICAL CHARACTERISTICS

High Speed ESD Lines: Dx, CLKx

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
I_{IO}	Current through ESD clamp ports	$V_{CCA} = 3.3\text{ V}$, $V_{CC5V} = 5.0\text{ V}$, $V_{IO} = 3.3\text{ V}$	D, CLK		0.01	0.5	μA
V_{DL}	Diode forward voltage	$I_D = 8\text{ mA}$	Lower clamp diode		0.8	1.0	V
R_{DYN}	Dynamic Resistance	$I = 1\text{ A}$	D, CLK		1		Ω
C_{IO}	IO capacitance	$V_{CC} = 5\text{ V}$, $V_{IO} = 2.5\text{ V}$	D, CLK		1.0		pF
ΔC_{IO_TMDS}	Differential capacitance for the Dx+, Dx- lines	$V_{CC} = 5\text{ V}$, $V_{IO} = 2.5\text{ V}$	D, CLK		0.05		pF
V_{BR}	Break-down Voltage	$I_{IO} = 1\text{ mA}$		6.5		9	V

Load Switch VCC5V, 5V_OUT

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I _{CC5V}	Supply current at VCC5V	VCC5V = 5V, 5V_OUT = Open, LS_OE = GND, CT_HPDP = 3.3V		1	45	μA
	Supply current at VCC5V	VCC5V = 5V, 5V_OUT = Open, LS_OE = GND, CT_HPDP = 3.3V		4	50	μA
I _{SC}	Short circuit current at 5V_OUT	VCC5V = 5V, 5V_OUT = GND	100	150	200	mA
V _{DROP}	5V_OUT output voltage drop	VCC5V = 5V, I _{5V_OUT} = 55 mA		35	50	mV
T _{ON}	Turn on Time, VCC5V to 5V_OUT	C _{LOAD} = 0.1 μF, R _{LOAD} = 500 Ω		77		μs
T _{OFF}	Turn off Time, VCC5V to 5V_OUT	C _{LOAD} = 0.1 μF, R _{LOAD} = 500 Ω		7.0		μs
T _{SHUT}	Thermal Shutdown	Shutdown threshold, TRIP ⁽¹⁾		140		°C
		HYST ⁽²⁾		12		

(1) The TPD12S016 turns off after the device temperature reaches the TRIP temperature.

(2) Once the thermal shut-down circuit turns off the load switch, the switch turns on again after the device junction temperature cools down to a temperature equals to or less than TRIP-HYST.

Voltage Level Shifter – SCL, SDA Lines (x_A and x_B Ports)

PARAMETER		TEST CONDITIONS		V _{CCA}	–40°C to 85°C			UNIT
					MIN	TYP	MAX	
V _{OHA}		I _{OH} = –20 μA	V _I = V _{IH}	1.1 V to 3.6 V	V _{CCA} × 0.80			V
V _{OLA}		I _{OL} = 20 μA	V _I = V _{IL}	1.1 V to 3.6 V	V _{CCA} × 0.17			V
V _{OHB}		I _{OH} = –20 μA	V _I = V _{IH}		5VOUT × 0.90			V
V _{OLB}		I _{OL} = 3 mA	V _I = V _{IL}		0.4			V
ΔV _T	Hysteresis at the SDx_A (V _{T+} – V _{T–})			1.1 V to 3.6 V	40			mV
ΔV _T	Hysteresis at the SDx_B (V _{T+} – V _{T–})			1.1 V to 3.6 V	400			mV
R _{PU}	(Internal pull-up)	SCL_A, SDA_A	Pull-up connected to VCCA rail		10			kΩ
		SCL_B, SDA_B	Pull-up connected to 5 V rail		1.75			
I _{PULLUP AC}	Transient boosted pull-up current (rise-time accelerator)	SCL_B, SDA_B	Pull-up connected to 5 V rail		15			mA
I _{off}	A port	VCCA = 0 V, V _I or V _O = 0 to 3.6 V		0 V	±5			μA
	B port	5VOUT = 0 V, V _I or V _O = 0 to 5.5 V		0 V to 3.6 V	±5			
I _{OZ}	B port	V _O = V _{CCO} or GND		1.1 V to 3.6 V	±5			μA
	A port	V _I = V _{CCI} or GND		1.1 V to 3.6 V	±5			

TPD12S016

SLLSE96A – SEPTEMBER 2011 – REVISED OCTOBER 2011

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Voltage Level Shifter – CEC Line (x_A and x_B ports)

PARAMETER		TEST CONDITIONS		V _{CCA}	–40°C to 85°C			UNIT
					MIN	TYP	MAX	
V _{OHA}		I _{OH} = –20 µA	V _I = V _{IH}	1.1 V to 3.6 V	V _{CCA} × 0.80			V
V _{OLA}		I _{OL} = 20 µA	V _I = V _{IL}	1.1 V to 3.6 V	V _{CCA} × 0.17			V
V _{OHB}		I _{OH} = –20 µA	V _I = V _{IH}		V _{3P3} × 0.80			V
V _{OLB}		I _{OL} = 3 mA	V _I = V _{IL}		0.4			V
ΔV _T	Hysteresis at the Sxx_A (V _{T+} – V _{T–})			1.1 V to 3.6 V	40			mV
ΔV _T	Hysteresis at the Sxx_B (V _{T+} – V _{T–})			1.1 V to 3.6 V	300			mV
R _{PU}	(Internal pull-up)	CEC_A	Pull-up connected to VCCA rail		10			kΩ
		CEC_B	Pull-up connected to 3.3 V rail		22	26	30	
I _{off}	A port	VCCA = 0 V, V _I or V _O = 0 to 3.6 V		0 V	±5			µA
	B port	5VOUT = 0 V, V _I or V _O = 0 to 5.5 V		0 V to 3.6 V	±1.8			
I _{OZ}	B port	V _O = V _{CCO} or GND		1.1 V to 3.6 V	±5			µA
	A port	V _I = V _{CCI} or GND		1.1 V to 3.6 V	±5			

Voltage Level Shifter – HPD Line (x_A and x_B ports)

PARAMETER		TEST CONDITIONS		V _{CCA}	–40°C to 85°C			UNIT
					MIN	TYP	MAX	
V _{OHA}		I _{OH} = –3 mA	V _I = V _{IH}	1.1 V to 3.6 V	V _{CCA} × 0.07			V
V _{OLA}		I _{OL} = 3 mA	V _I = V _{IL}	1.1 V to 3.6 V	0.4			V
ΔV _T	Hysteresis (V _{T+} – V _{T–})			1.1 V to 3.6 V	400			mV
R _{PD}	(Internal pull-down resistor)	HPD_B	Pull-down connected to GND		11			kΩ
I _{off}	A port	V _O = V _{CCO} or GND		0 V	±5			µA
I _{OZ}	A port	V _I = V _{CCO} or GND		3.6 V	±5			µA

LS_OE, CT_CP_HPDP

PARAMETER	TEST CONDITIONS	V _{CCA}	–40°C to 85°C			UNIT
			MIN	TYP	MAX	
I _I	V _I = V _{CCA} or GND	1.1 V to 3.6 V	±12			µA

I/O Capacitances

PARAMETER		TEST CONDITIONS	V _{CCA}	–40°C to 85°C			UNIT
				MIN	TYP	MAX	
C _I	Control inputs	V _I = 1.89 V or GND	1.1 V to 3.6 V	7.1			pF
C _{io}	A port	V _O = 1.89 V or GND	1.1 V to 3.6 V	8.3			pF
	B port	V _O = 5.0 V or GND	5.0 V	15			pF

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _L	Bus Load Capacitance (B Side)				750	pF
	Bus Load Capacitance (A Side)				15	

Voltage Level Shifter – SCL, SDA Lines (x_A and x_B ports) VCCA = 1.2 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		310		nS
		B to A	SCL/SDA Channels Enabled		420		
t _{PLH}	Propagation delay	A to B	SCL/SDA Channels Enabled		510		nS
		B to A	SCL/SDA Channels Enabled		427		
t _{FALL}	A Port fall time	A-Port	SCL/SDA Channels Enabled		334		nS
	B Port fall time	B-Port	SCL/SDA Channels Enabled		225		
t _{RISE}	A Port rise time	A-Port	SCL/SDA Channels Enabled		315		nS
	B Port rise time	B-Port	SCL/SDA Channels Enabled		415		
F _(MAX)	Maximum switching frequency		SCL/SDA Channels Enabled	400			kHz

Voltage Level Shifter – CEC Lines (x_A and x_B ports) VCCA = 1.2 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	CEC Channel Enabled		385		nS
		B to A	CEC Channel Enabled		526		
t _{PLH}	Propagation delay	A to B	CEC Channel Enabled		13.8		μS
		B to A	CEC Channel Enabled		16.6		
t _{FALL}	A Port fall time	A-Port	CEC Channel Enabled		334		nS
	B Port fall time	B-Port	CEC Channel Enabled		170		
t _{RISE}	A Port rise time	A-Port	CEC Channel Enabled		315		nS
	B Port rise time	B-Port	CEC Channel Enabled		28		

Voltage Level Shifter – HPD Lines (x_A and x_B ports) VCCA = 1.2 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	B to A	HPD Channel Enabled		14.4		μS
t _{PLH}	Propagation delay	B to A	HPD Channel Enabled		9.2		μS
t _{FALL}	A Port fall time	A-Port	HPD Channel Enabled		2.1		nS
t _{RISE}	A Port rise time	A-Port	HPD Channel Enabled		2.1		nS

Voltage Level Shifter – SCL, SDA Lines (x_A and x_B ports) VCCA = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		310		nS
		B to A	SCL/SDA Channels Enabled		420		
t _{PLH}	Propagation delay	A to B	SCL/SDA Channels Enabled		410		nS
		B to A	SCL/SDA Channels Enabled		425		
t _{FALL}	A Port fall time	A-Port	SCL/SDA Channels Enabled		250		nS
	B Port fall time	B-Port	SCL/SDA Channels Enabled		225		
t _{RISE}	A Port rise time	A-Port	SCL/SDA Channels Enabled		315		nS
	B Port fall time	B-Port	SCL/SDA Channels Enabled		415		
F _(MAX)	Maximum switching frequency		SCL/SDA Channels Enabled	400			kHz

TPD12S016

SLLSE96A – SEPTEMBER 2011 – REVISED OCTOBER 2011

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Voltage Level Shifter – CEC Lines (x_A and x_B ports) VCCA = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	CEC Channel Enabled		380		nS
		B to A	CEC Channel Enabled		420		
t _{PLH}	Propagation delay	A to B	CEC Channel Enabled		13.8		μS
		B to A	CEC Channel Enabled		16.6		nS
t _{FALL}	A Port fall time	A-Port	CEC Channel Enabled		250		nS
	B Port fall time	B-Port	CEC Channel Enabled		170		
t _{RISE}	A Port rise time	A-Port	CEC Channel Enabled		315		nS
	B Port rise time	B-Port	CEC Channel Enabled		28		μS

Voltage Level Shifter – HPD Lines (x_A and x_B ports) VCCA = 1.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	B to A	HPD Channel Enabled		14.4		μS
t _{PLH}	Propagation delay	B to A	HPD Channel Enabled		9.2		μS
t _{FALL}	A Port fall time	A-Port	HPD Channel Enabled		1.8		nS
t _{RISE}	A Port rise time	A-Port	HPD Channel Enabled		1.8		nS

Voltage Level Shifter – SCL, SDA Lines (x_A and x_B ports) VCCA = 1.8 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		300		nS
		B to A	SCL/SDA Channels Enabled		350		
t _{PLH}	Propagation delay	A to B	SCL/SDA Channels Enabled		400		nS
		B to A	SCL/SDA Channels Enabled		420		
t _{FALL}	A Port fall time	A-Port	SCL/SDA Channels Enabled		210		nS
	B Port fall time	B-Port	SCL/SDA Channels Enabled		225		
t _{RISE}	A Port rise time	A-Port	SCL/SDA Channels Enabled		315		nS
	B Port fall time	B-Port	SCL/SDA Channels Enabled		415		
F _(MAX)	Maximum switching frequency		SCL/SDA Channels Enabled	400			kHz

Voltage Level Shifter – CEC Lines (x_A and x_B ports) VCCA = 1.8 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	CEC Channel Enabled		375		nS
		B to A	CEC Channel Enabled		366		
t _{PLH}	Propagation delay	A to B	CEC Channel Enabled		13.8		μS
		B to A	CEC Channel Enabled		16.6		
t _{FALL}	A Port fall time	A-Port	CEC Channel Enabled		210		nS
	B Port fall time	B-Port	CEC Channel Enabled		170		
t _{RISE}	A Port rise time	A-Port	CEC Channel Enabled		315		nS
	B Port rise time	B-Port	CEC Channel Enabled		28		

Voltage Level Shifter – HPD Lines (x_A and x_B ports) VCCA = 1.8 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	B to A	HPD Channels Enabled		14.2		μS
t _{PLH}	Propagation delay	B to A	HPD Channel Enabled		9.2		μS
t _{FALL}	A Port fall time	A-Port	HPD Channel Enabled		1.5		nS
t _{RISE}	A Port rise time	A-Port	HPD Channel Enabled		1.5		nS

Voltage Level Shifter – SCL, SDA Lines (x_A and x_B ports) VCCA = 2.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		300		nS
		B to A	SCL/SDA Channels Enabled		400		nS
t _{PLH}	Propagation delay	A to B	SCL/SDA Channels Enabled		290		nS
		B to A	SCL/SDA Channels Enabled		420		nS
t _{FALL}	A Port fall time	A-Port	SCL/SDA Channels Enabled		170		nS
	B Port fall time	B-Port	SCL/SDA Channels Enabled		225		nS
t _{RISE}	A Port rise time	A-Port	SCL/SDA Channels Enabled		315		nS
	B Port fall time	B-Port	SCL/SDA Channels Enabled		415		nS
F _(MAX)	Maximum switching frequency		SCL/SDA Channels Enabled	400			kHz

Voltage Level Shifter – CEC Lines (x_A and x_B ports) VCCA = 2.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	CEC Channel Enabled		375		nS
		B to A	CEC Channel Enabled		305		
t _{PLH}	Propagation delay	A to B	CEC Channel Enabled		13.8		μS
		B to A	CEC Channel Enabled		16.6		nS
t _{FALL}	A Port fall time	A-Port	CEC Channel Enabled		170		nS
	B Port fall time	B-Port	CEC Channel Enabled		170		
t _{RISE}	A Port rise time	A-Port	CEC Channel Enabled		315		nS
	B Port rise time	B-Port	CEC Channel Enabled		28		μS

Voltage Level Shifter – HPD Lines (x_A and x_B ports) VCCA = 2.5 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	B to A	HPD Channel Enabled		14.2		μS
t _{PLH}	Propagation delay	B to A	HPD Channel Enabled		9.2		μS
t _{FALL}	A Port fall time	A-Port	HPD Channel Enabled		1.2		nS
t _{RISE}	A Port rise time	A-Port	HPD Channel Enabled		1.2		nS

Voltage Level Shifter – SCL, SDA Lines (x_A and x_B ports) VCCA = 3.3 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	SCL/SDA Channels Enabled		300		nS
		B to A	SCL/SDA Channels Enabled		400		nS
t _{PLH}	Propagation delay	A to B	SCL/SDA Channels Enabled		260		nS
		B to A	SCL/SDA Channels Enabled		415		nS
t _{FALL}	A Port fall time	A-Port	SCL/SDA Channels Enabled		160		nS
	B Port fall time	B-Port	SCL/SDA Channels Enabled		225		nS
t _{RISE}	A Port rise time	A-Port	SCL/SDA Channels Enabled		305		nS
	B Port fall time	B-Port	SCL/SDA Channels Enabled		415		nS
F _(MAX)	Maximum switching frequency		SCL/SDA Channels Enabled	400			kHz

TPD12S016

SLLSE96A – SEPTEMBER 2011 – REVISED OCTOBER 2011

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Voltage Level Shifter – CEC Lines (x_A and x_B ports) VCCA = 3.3 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	A to B	CEC Channel Enabled		375		nS
		B to A	CEC Channel Enabled		305		
t _{PLH}	Propagation delay	A to B	CEC Channel Enabled		13.8		μS
		B to A	CEC Channel Enabled		16.6		nS
t _{FALL}	A Port fall time	A-Port	CEC Channel Enabled		160		nS
	B Port fall time	B-Port	CEC Channel Enabled		170		
t _{RISE}	A Port rise time	A-Port	CEC Channel Enabled		305		nS
	B Port rise time	B-Port	CEC Channel Enabled		28		μS

Voltage Level Shifter – HPD Lines (x_A and x_B ports) VCCA = 3.3 V

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay	B to A	HPD Channel Enabled		14.2		μS
t _{PLH}	Propagation delay	B to A	HPD Channel Enabled		9.2		μS
t _{FALL}	A Port fall time	A-Port	HPD Channel Enabled		1.1		nS
t _{RISE}	A Port rise time	A-Port	HPD Channel Enabled		1.1		nS

APPLICATION INFORMATION

DDC/CEC LEVEL SHIFT Circuit Operation

The TPD12S016 enables DDC translation from VCCA (system side) voltage levels to 5V (HDMI cable side) voltage levels without degradation of system performance. The TPD12S016 contains 2 bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage, VCCA side DDC-bus and the 5V DDC-bus. The port B I/Os are over-voltage tolerant to 5.5 V even when the device is un-powered. After power-up and with the LS_OE and CT_HPDP pins HIGH, a LOW level on port A (below approximately $V_{ILC} = 0.08 \times V_{CCA}$ V) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to V_{OLB} V. When port A rises above approximately $0.10 \times V_{CCA}$ V, the port B pull-down driver is turned off and the internal pull-up resistor pulls the pin HIGH. When port B falls first and goes below $0.3 \times 5V_{OUT}$, a CMOS hysteresis input buffer detects the falling edge, turns on the port A driver, and pulls port A down to approximately $V_{OLA} = 0.16 \times V_{CCA}$ V. The port B pull-down is not enabled unless the port A voltage goes below V_{ILC} . If the port A low voltage goes below V_{ILC} , the port B pull-down driver is enabled until port A rises above $(V_{ILC} + \Delta V_{T-HYSTA})$, then port B, if not externally driven LOW, will continue to rise being pulled up by the internal pull-up resistor.

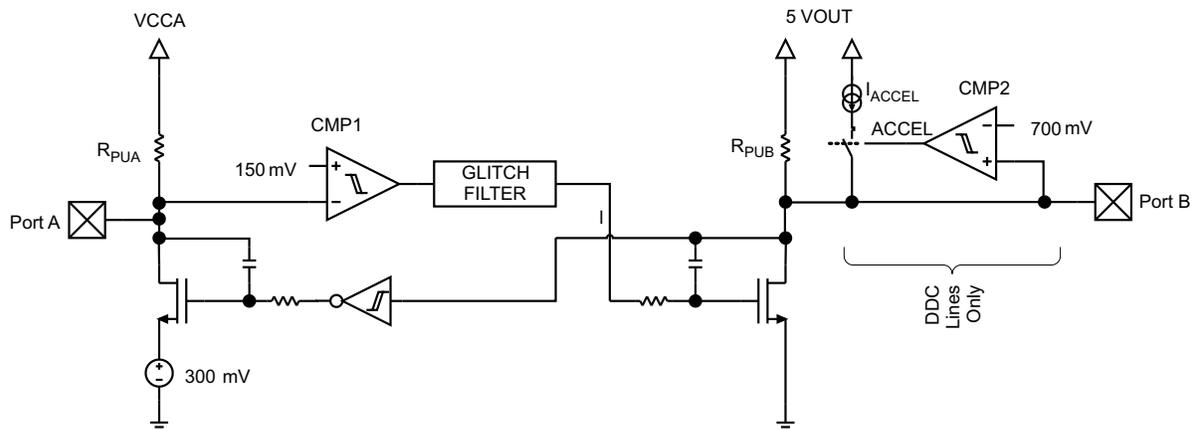


Figure 3. DDC/CEC Level Shifter Block Diagram

DDC/CEC Level Shifter Operational Notes for VCCA=1.8V

- The threshold of CMP1 is $\sim 150\text{mV} \pm$ the 40mV of total hysteresis.
- The comparator will trip for a falling waveform at $\sim 130\text{mV}$
- The comparator will trip for a rising waveform at $\sim 170\text{mV}$
- To be recognized as a zero, the level at Port A must first go below 130mV (V_{ILC} in spec) and then stay below 170mV (V_{ILA} in spec)
- To be recognized as a one, the level at A must first go above 170mV and then stay above 130mV
- V_{ILC} is set to 110mV in Electrical Characteristics Table to give some margin to the 130mV
- V_{ILA} is set to 140mV in the Electrical Characteristics Table to give some margin to the 170mV
- V_{IHA} is set to 70% of VCCA to be consistent with standard CMOS levels

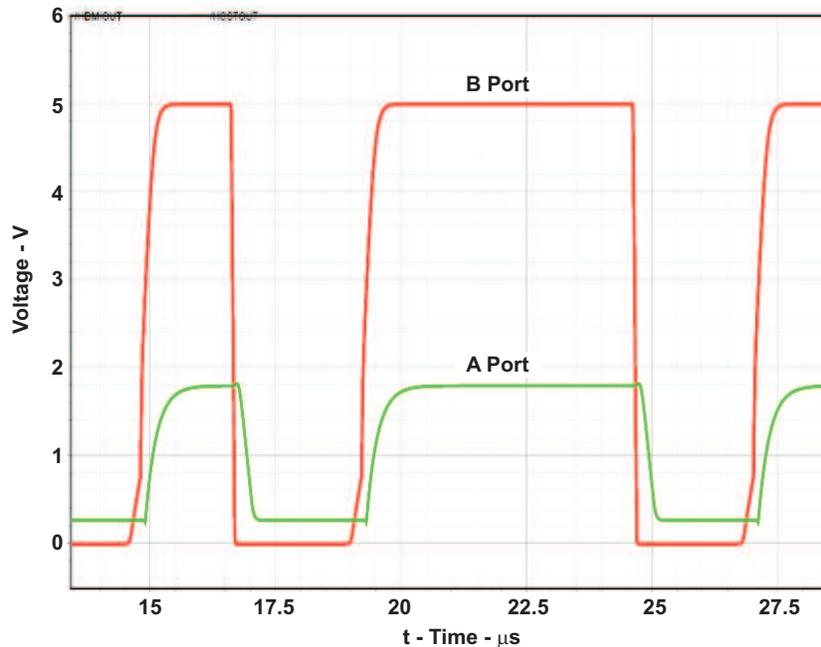


Figure 4. DDC Level Shifter Operation (B to A Direction)

Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support the high capacitive load on the HDMI cable side. The rise time accelerator boosts the cable side DDC signal independent of which side of the bus is releasing the signal.

Noise Considerations:

Ground offset between the TPD12S016 ground and the ground of devices on port A of the TPD12S016 must be avoided. The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133 Ω or less ($R = E / I$). Such a driver will share enough current with the port A output pull-down of the TPD12S016 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{ILC} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the port A of the TPD12S016 as their output LOW levels will not be recognized by the TPD12S016 as a LOW. If the TPD12S016 is placed in an application where the V_{IL} of port A of the TPD12S016 does not go below its V_{ILC} it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it will not reproduce the port A input on port B. Such applications should be avoided. Port B is interoperable with all I2C-bus slaves, masters and repeaters.

Resistor Pull-Up Value Selection

The system is designed to work properly with no external pull-up resistors on the DDC, CEC, and HPD lines.

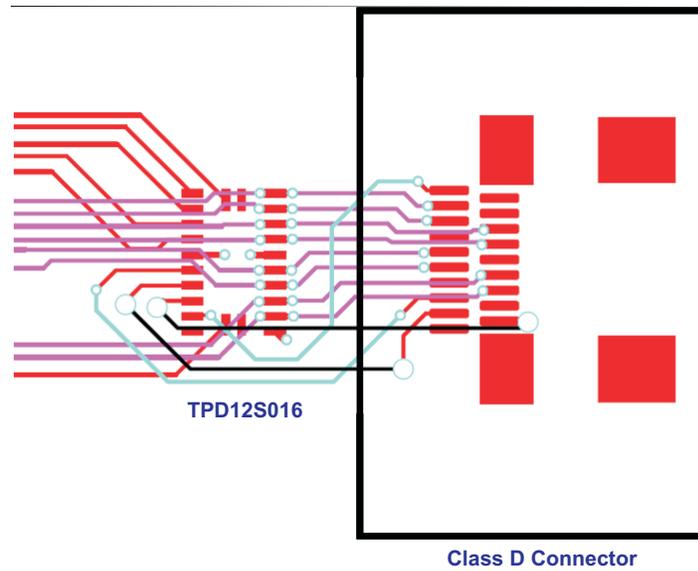


Figure 5. Board Layout for RKT Package

TYPICAL CHARACTERISTICS

IEC CLAMPING WAVEFORM
+8kV CONTACT

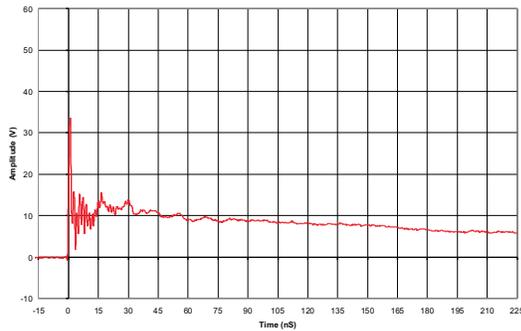


Figure 6.

IEC CLAMPING WAVEFORM
-8kV CONTACT

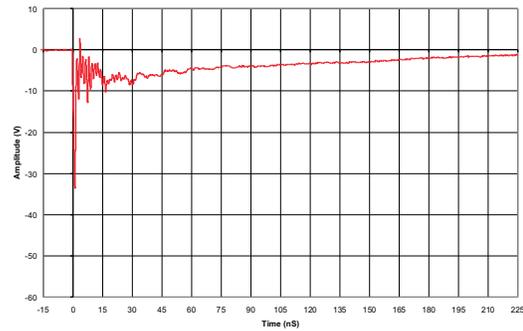


Figure 7.

CT_HPD V_{TH}

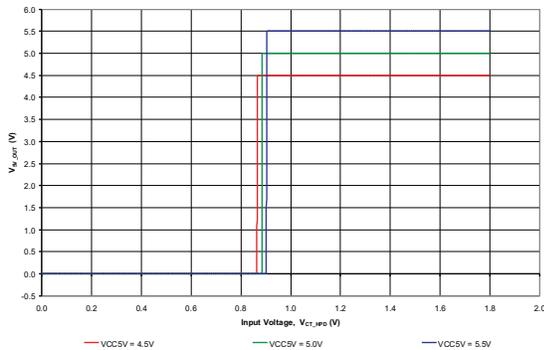


Figure 8.

INSERTION LOSS, DATA LINE TO GND

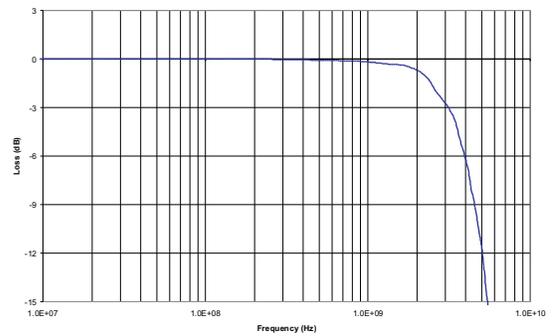


Figure 9.

CHANNEL-TO-CHANNEL CROSSTALK

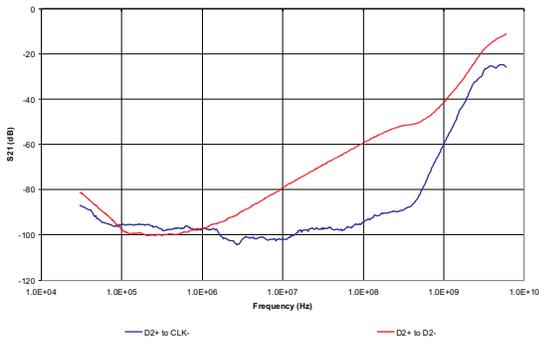


Figure 10.

SWITCH RESISTANCE vs TEMPERATURE
I_{SWITCH} ~ 55mA

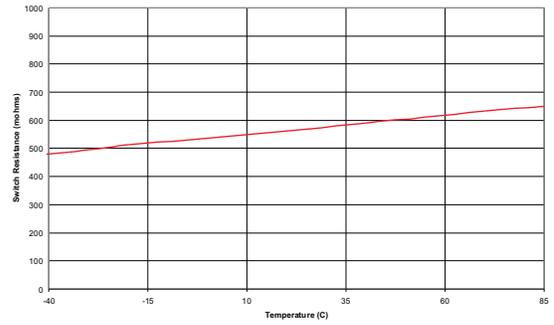


Figure 11.

I_{OUT} vs TEMPERATURE

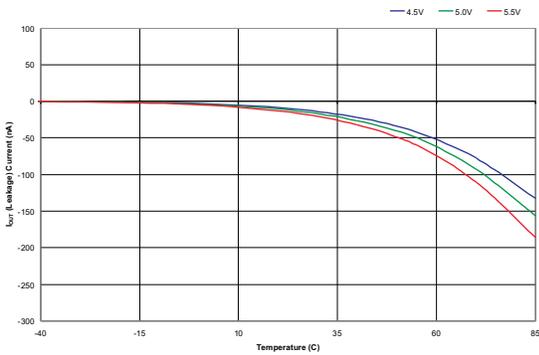


Figure 12.

I₀ vs TEMPERATURE

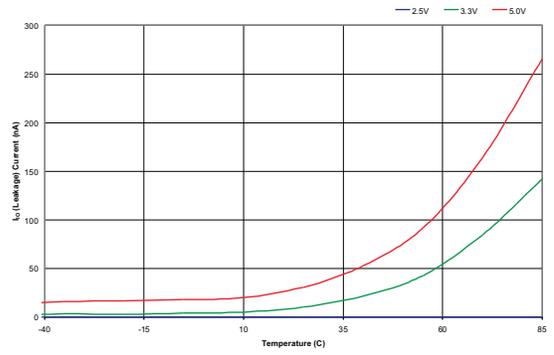


Figure 13.

SHORT-CIRCUIT RESPONSE TIME
(POWERED-UP TO SHORT)

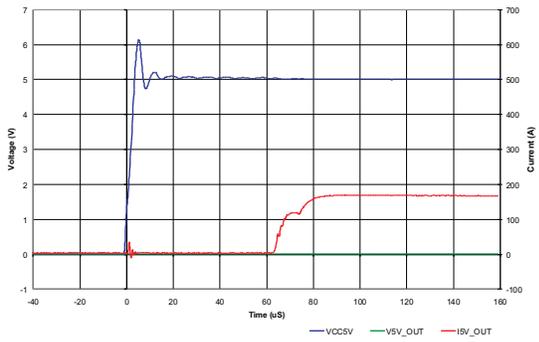


Figure 14.

CURRENT LIMIT RESPONSE TIME
(SWITCH ENABLED TO SHORT)

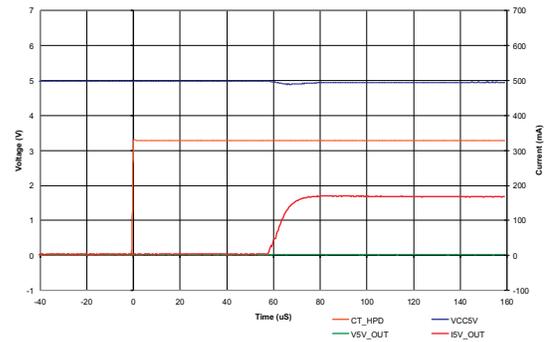


Figure 15.

CAPACITANCE vs BIAS VOLTAGE

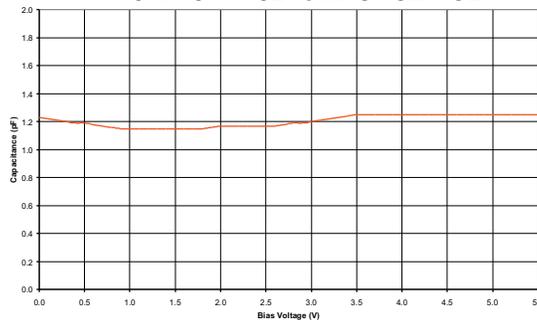


Figure 16.

Eye Diagram Using EVM Without TPD12S016 for the TMDS Lines at 1080p, 340MHz Pixel Clock, 3.4Gbps

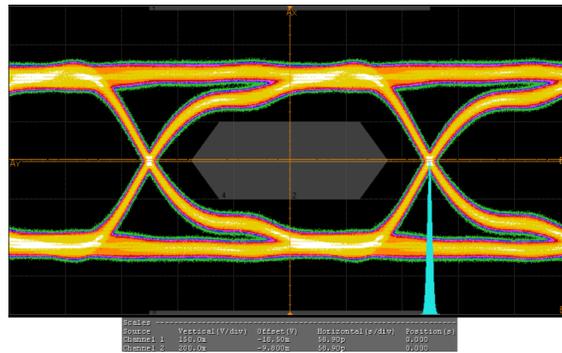


Figure 17.

Eye Diagram Using EVM with TPD12S016 for the TMDS Lines at 1080p, 340MHz Pixel Clock, 3.4Gbps

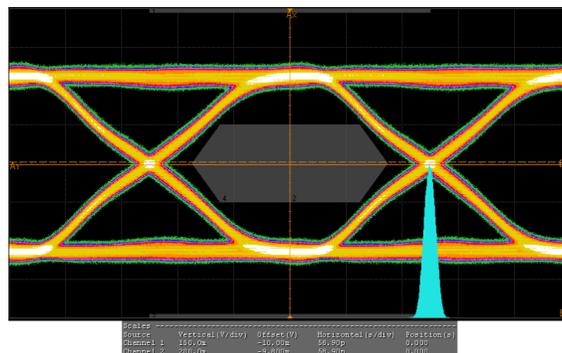


Figure 18.

REVISION HISTORY

Changes from Original (September 2011) to Revision A	Page
• Added Eye Diagram Using EVM Without TPD12S016 for the TMDS Lines at 1080p, 340MHz Pixel Clock, 3.4Gbps	17
• Added Eye Diagram Using EVM with TPD12S016 for the TMDS Lines at 1080p, 340MHz Pixel Clock, 3.4Gbps	17

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TPD12S016PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPD12S016RKTR	PREVIEW	UQFN	RKT	24	3000	TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

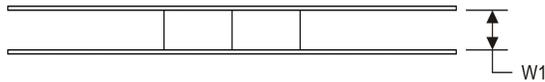
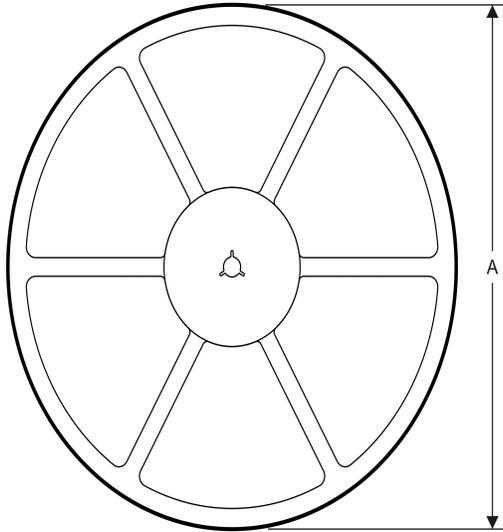
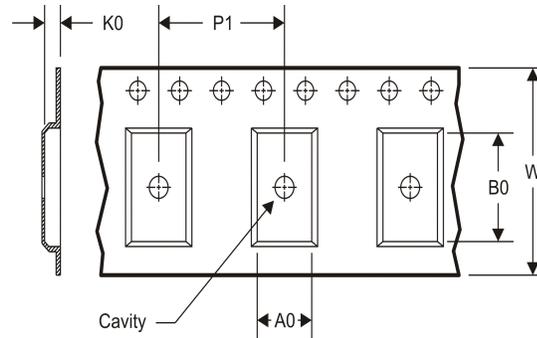
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


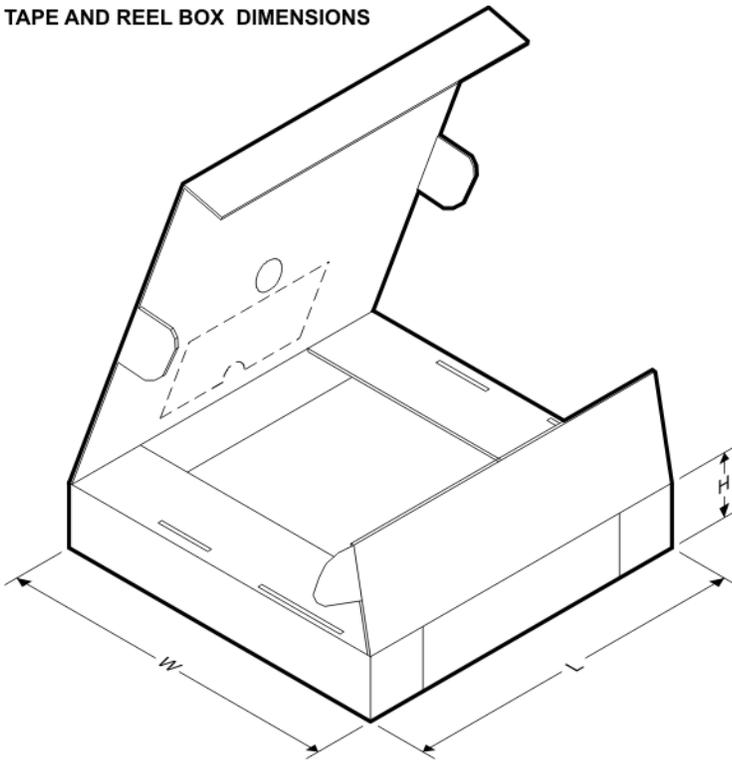
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD12S016PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

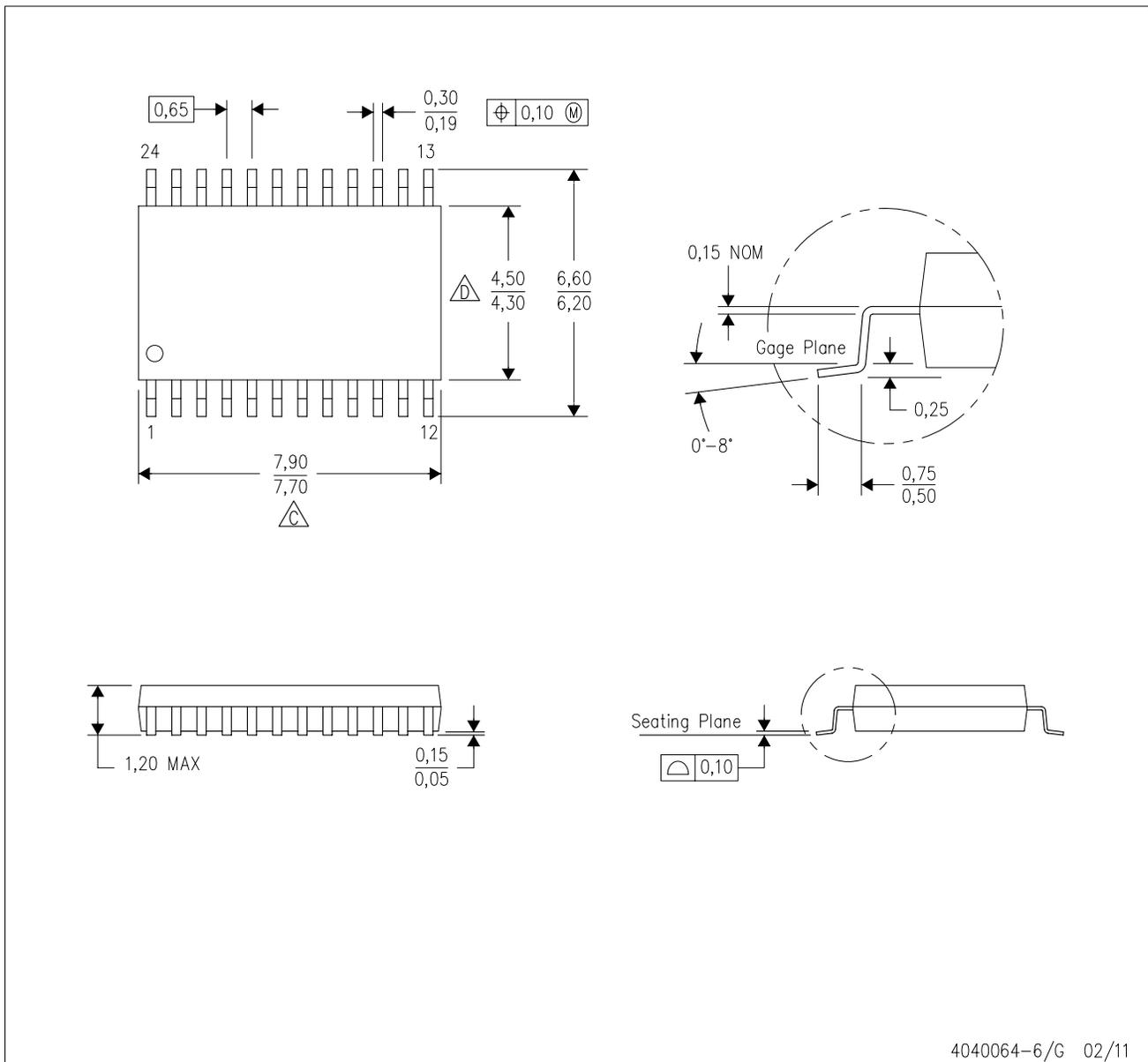


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD12S016PWR	TSSOP	PW	24	2000	346.0	346.0	33.0

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

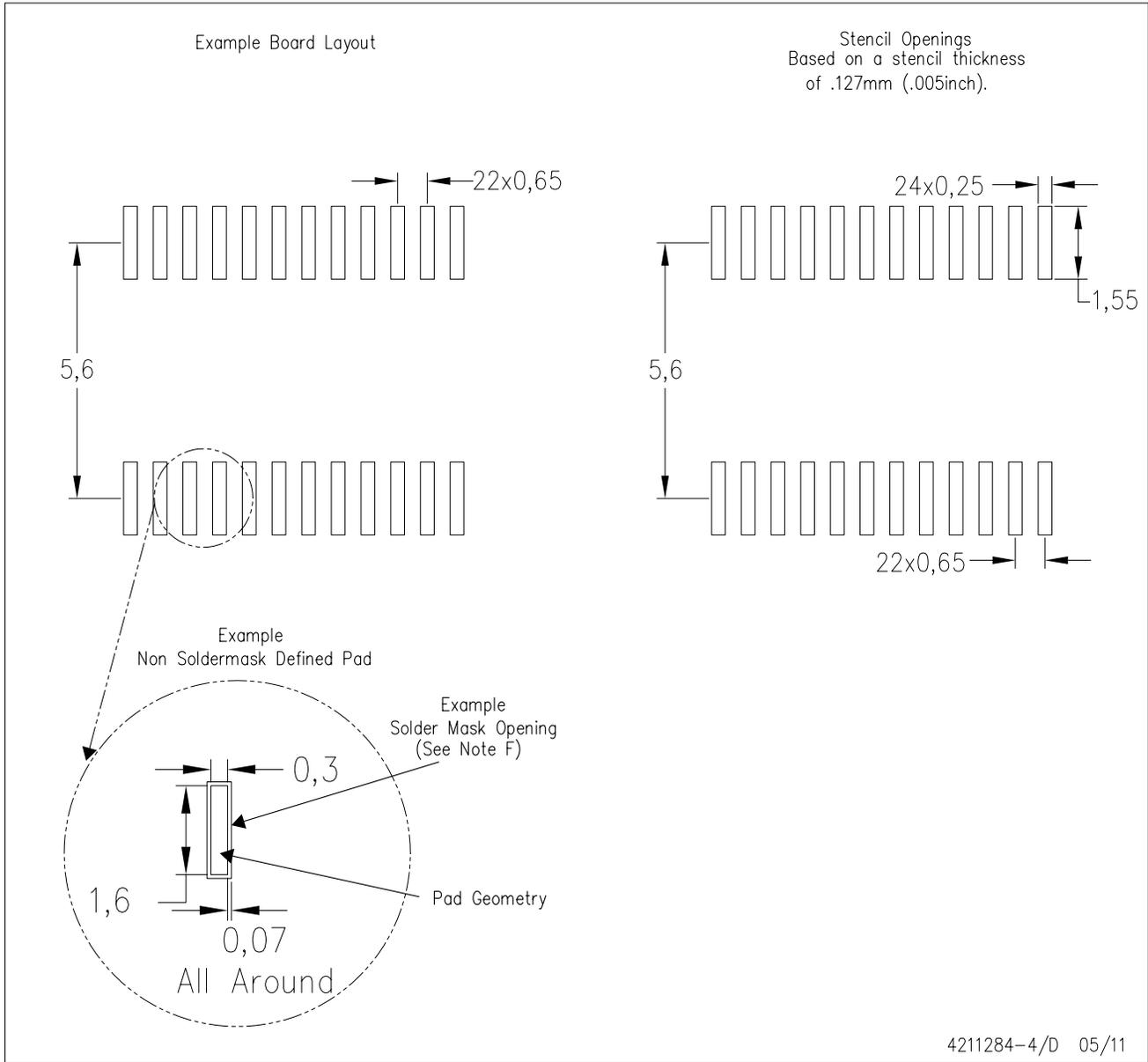


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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